Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of operating a processor comprising:

executing a branch instruction in execution of an instruction stream with a branch based on a bit ~~specified in the branch instruction~~ of a register ~~specified in the branch instruction~~ being set or cleared, the bit and the register being specified in the branch instruction, and including a first token that specifies the number of instructions in the instruction stream that are after the branch instruction to execute before performing the branch operation and a second token that specifies a branch guess operation.

2. (Previously presented) The method of claim 1 wherein the second token that specifies the branch guess operation if set, pre-fetches a guessed instruction.

3. (Previously presented) The method of claim 1 wherein the branch instruction further comprises an optional token that indicates a pipeline stage that the branch operation is evaluated in.

4. (Previously presented) The method of claim 1 wherein the first token can specify, one, two or three instructions following to execute before performing the branch operation.

5. (Cancelled).

6. (Previously presented) The method of claim 1 wherein one the tokens are specified by a programmer or assembler program to enable variable cycle deferred branching.